What is claimed is:

1. A CMOS thin film transistor, comprising: an active channel of a P-type thin film transistor, the active channel being formed in polycrystalline silicon, an active channel of a N-type thin film transistor, the active channel being formed in polycrystalline silicon, primary grain boundaries in the P-type thin film transistor, primary grain boundaries in the N-type thin film transistor, wherein a direction of the active channel of the P-type transistor is different from a direction of the active channel of the N-type transistor such that the primary grain boundaries of the P-type thin film transistor are at an angle of about 60° to about 120° with respect to the active channel direction of the P-type thin film transistor and the primary grain boundaries of the N-type thin film transistor are out an angle of about -30° to about 30° with respect to the active channel direction of the N-type thin film transistor.

2. The CMOS thin film transistor of claim 1, wherein the P-type thin film transistor is formed such that it has a low current mobility while the N-type thin film transistor is formed such that it has a high current mobility.

3. The CMOS thin film transistor of claim 1, wherein the P-type thin film transistor is formed such that it has a low threshold voltage while the N-type thin film transistor is formed such that it has a high threshold voltage.

4. The CMOS thin film transistor of claim 3, wherein a difference between an absolute value of the threshold voltage of the P-type thin film transistor and an absolute value of the threshold voltage of the N-type thin film transistor is 0.

5. The CMOS thin film transistor of claim 3, wherein a difference between an absolute value of the threshold voltage of the P-type thin film transistor and an absolute value of the threshold voltage of the N-type thin film transistor is substantially zero.

6. The CMOS thin film transistor of claim 1, wherein a length of a channel of the P-type thin film transistor is substantially equal to a length of a channel of the N-type thin film transistor.

7. The CMOS thin film transistor of claim 1, wherein the polycrystalline silicon is fabricated by a sequential lateral solidification (SLS) crystallization method.

8. The CMOS thin film transistor of claim 1, wherein the primary grain boundaries of the P-type thin film transistor are substantially perpendicular to an active channel direction of the P-type thin film transistor, and the primary grain boundaries of the N-type thin film transistor are substantially horizontal to the active channel direction of the N-type thin film transistor.

9. The CMOS thin film transistor of claim 1, wherein the primary grain boundaries of the P-type thin film transistor are perpendicular to an active channel direction of the P-type thin film transistor, and the primary grain boundaries of the N-type thin film transistor are horizontal to the active channel direction of the N-type thin film transistor.

10. The CMOS thin film transistor of claim 1, wherein a majority of the primary grain boundaries of the P-type thin film transistor are substantially perpendicular to an active channel direction of the P-type thin film transistor, and a majority of the primary grain boundaries of the N-type thin film transistor are substantially horizontal to the active channel direction of the N-type thin film transistor.

11. The CMOS thin film transistor of claim 1, wherein the CMOS thin film transistor includes a lightly doped drain (LDD) structure or off set structure.

12. A display device, comprising:

a CMOS thin film transistor, the CMOS thin film transistor comprising:

an active channel of a P-type thin film transistor, the active channel being formed in polycrystalline silicon,

an active channel of a N-type thin film transistor, the active channel being formed in polycrystalline silicon, primary grain boundaries in the P-type thin film transistor,

primary grain boundaries in the N-type thin film transistor, wherein a direction of the active channel of the P-type transistor is different from a direction of the active channel of the N-type transistor such that the primary grain boundaries of the P-type thin film transistor are at an angle of about 60° to about 120° with respect to the active channel direction of the P-type thin film transistor and the primary grain boundaries of the N-type thin film transistor are out an angle of about -30° to about 30° with respect to the active channel direction of the N-type thin film transistor.

13. The display device of claim 12, wherein the display device is a liquid crystal display (LCD) device or an organic electroluminescent display device.

14. A method of fabricating a CMOS thin film transistor, the method comprising:

forming a polysilicon pattern for a N-type thin film transistor and a polysilica pattern for a P-type thin film transistor on a substrate by crystallizing amorphous silicon using a laser whereby grain boundaries between grains are formed in the polysilicon pattern for the N-type thin film transistor and the polysilica pattern for the P-type thin film transistor,

wherein an angle between grain boundaries of the N-type thin film transistor and an active channel region of the N-type thin film transistor is about -30° to about 30° and an angle between grain boundaries of the P-type thin film transistor and an active channel of the P-type thin film transistor is about 60° to about 120°.

15. The method of fabricating a CMOS thin film transistor of claim 14, wherein the angle between the grain boundaries of the N-type thin film transistor and the active channel of the N-type thin film transistor is substantially equal to zero and the angle between the grain boundaries of the P-type thin film transistor and the active channel of the P-type think film transistor is substantially equal to 90°.